

**A CAPACITOR FORMED ON A RECRYSTALLIZED  
POLYSILICON LAYER AND A METHOD OF MANUFACTURE THEREFOR**

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**TECHNICAL FIELD OF THE INVENTION**

[0001] The present invention is directed, in general, to a semiconductor device and, more specifically, to a capacitor formed on a recrystallized polysilicon layer and a method of manufacture therefor.

**BACKGROUND OF THE INVENTION**

[0002] Modern electronic equipment such as televisions, telephones, radios and computers are generally constructed of solid state devices. Solid state devices are preferred in electronic equipment because they are extremely small and relatively inexpensive. Additionally, solid state devices are very reliable because they have no moving parts, but are based on the movement of charge carriers.

[0003] Solid state devices may be transistors, capacitors, resistors and other semiconductor devices. Typically, such devices are fabricated on a substrate and interconnected to form memory arrays, logic structures, timers and other integrated circuits. One type of memory array is a dynamic random access memory (DRAM) in

which memory cells retain information only temporarily and are refreshed at periodic intervals. Despite this limitation, DRAMs are widely used because they provide low cost per bit of memory, high device density and feasibility of use.

[0004] In a DRAM, each memory cell typically includes an access transistor coupled to a storage capacitor. In order to fabricate high density DRAMs, the storage capacitors must take up less planar area in the memory cells. As storage capacitors are scaled down in dimensions, a sufficiently high storage capacity must be maintained. Efforts to maintain storage capacity have concentrated on building three-dimensional capacitor structures that increase the capacitor surface area. The increased surface area provides for increased storage capacity. Three-dimensional capacitor structures typically include trench capacitors and stacked capacitors. While trench capacitors are still used, many of the capacitors currently used are of the stacked capacitor type.

[0005] Stacked capacitors typically include first and second conductive electrodes separated by an insulative material. Often the first, or lower electrode, comprises a material such as cobalt silicide, the insulative material comprises a material such as silicon dioxide, and the second, or upper electrode, comprises a material such as titanium nitride. This is particularly the case when striving for high performance capacitors.

[0006] While the above-discussed capacitors are used as high

performance capacitors, their use is not without certain drawbacks. One such drawback stems from the difficulty in forming substantially planar first, or lower electrodes. Specifically, the first, or lower electrodes, presently have varying and unpredictable amounts of roughness. This unfortunately, causes the capacitors to have varying and unpredictable amounts of capacitance, as a result of the increased or decreased surface area of the first, or lower electrode. It has been observed that the varying and unpredictable amounts of roughness are particularly evident when the first, or lower electrode, is formed over a polysilicon substrate. Unfortunately, these capacitors are often formed directly on the polysilicon gate of the underlying transistor, which exaggerates this problem.

[0007] Accordingly, what is needed in the art is a capacitor that does not experience the lower electrode roughness experienced by the prior art capacitors.

## SUMMARY OF THE INVENTION

[0008] To address the above-discussed deficiencies of the prior art, the present invention provides a semiconductor device, a method of manufacture therefor, and an integrated circuit including the semiconductor device. The semiconductor device, among other elements, includes a recrystallized polysilicon layer located over a gate electrode layer, and a capacitor located on the recrystallized polysilicon layer. The capacitor, in this embodiment, includes a first electrode, an insulator located over the first electrode, and a second electrode located over the insulator.

[0009] In addition to the semiconductor device, the present invention provides a method of manufacturing the semiconductor device. The method for manufacturing the semiconductor device includes forming an amorphous silicon layer over a substrate, then changing the amorphous silicon layer to a recrystallized polysilicon layer. The method further includes creating a capacitor on the recrystallized polysilicon layer, wherein the capacitor includes a first electrode, an insulator located over the first electrode, and a second electrode located over the insulator.

[0010] The present invention, as mentioned above, further includes an integrated circuit. The integrated circuit includes 1) transistors located over a substrate, wherein at least one of the

transistors includes a gate electrode stack comprising a recrystallized polysilicon layer located over a gate electrode layer, 2) a capacitor located on the recrystallized polysilicon layer, wherein the capacitor includes a first electrode, an insulator located over the first electrode, and a second electrode located over the insulator, and 3) an interlevel dielectric layer located over the substrate, the interlevel dielectric layer having interconnects located therein for contacting at least one of the gate electrode stack or the capacitor.

[0011] The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention is best understood from the following detailed description when read with the accompanying FIGURES. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0013] FIGURE 1A illustrates a cross-sectional view of one embodiment of a semiconductor device constructed according to the principles of the present invention;

[0014] FIGURE 1B illustrates an embodiment of the present invention wherein an additional layer, or layers, of material interpose the gate electrode layer and the recrystallized polysilicon layer;

[0015] FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device;

[0016] FIGURE 3 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 2 after formation of a gate structure over the substrate;

[0017] FIGURE 4 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 3

after formation of lightly doped extension implants within the substrate;

[0018] FIGURE 5 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 4 after formation of conventional gate sidewall spacers and after formation of highly doped source/drain implants within the substrate;

[0019] FIGURE 6 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 5 after subjecting it to a standard source/drain anneal thereby activating source/drain regions;

[0020] FIGURE 7 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 6 after depositing a first electrode layer on the recrystallized polysilicon layer;

[0021] FIGURE 8 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 7 after subjecting the first electrode layer of FIGURE 7 to a first rapid thermal anneal (RTA) process and a selective wet etch process;

[0022] FIGURE 9 illustrates a cross-sectional view of the partially completed semiconductor device illustrated in FIGURE 8 after subjecting the first electrode layer of FIGURE 8 to a second rapid thermal anneal (RTA) process;

[0023] FIGURE 10 illustrates sheet resistance ( $R_s$ ) and surface nonuniformity (NU%) for three different situations of devices;

[0024] FIGURE 11 illustrates a graph showing the surface roughness measured using an atomic force microscope (AFM) of samples similar to the three different situations illustrated in FIGURE 10;

[0025] FIGURE 12 illustrates a comparison of the inversion capacitance of a polysilicon gate electrode layer and a recrystallized polysilicon gate electrode layer; and

[0026] FIGURE 13 illustrates a cross-sectional view of a conventional integrated circuit (IC) incorporating devices constructed according to the principles of the present invention.

## DETAILED DESCRIPTION

[0027] Referring initially to FIGURE 1A, illustrated is a cross-sectional view of one embodiment of a semiconductor device 100 constructed according to the principles of the present invention. In the embodiment illustrated in FIGURE 1A, the semiconductor device 100 includes a substrate 110. Located within the substrate 110 in the embodiment of FIGURE 1A is a well region 120. Additionally, located over the substrate 110 and well region 120 is a gate structure 130.

[0028] The gate structure 130 illustrated in FIGURE 1A includes a gate oxide 135 located over the substrate 110, as well as a gate electrode stack 140 located over the gate oxide 135. In the particular embodiment shown, the gate electrode stack 140 includes a gate electrode layer 143, such as a polysilicon gate electrode, and a recrystallized polysilicon layer 148 located over the gate electrode layer 143. The recrystallized polysilicon layer 148 may have a final thickness that ranges from about 7 nm to about 35 nm, among others. Flanking both sides of the gate electrode stack 140 and gate oxide 135 of the gate structure 130 depicted in FIGURE 1A are gate sidewall spacers 150.

[0029] The semiconductor device 100 illustrated in FIGURE 1A further includes conventional source/drain regions 160 located within the substrate 110. The source/drain regions 160, as is

common, may each include a lightly doped extension implant 163 as well as a higher doped source/drain implant 168.

[0030] Located on the recrystallized polysilicon layer 148 of the gate electrode stack 140 is a capacitor 170. The capacitor 170, which often is a high performance capacitor, includes a first electrode 173, or in this instance a lower electrode, located on the recrystallized polysilicon layer 148. The capacitor 170 further includes an insulator 175 located over the first electrode 173, as well as a second electrode 178, or in this instance an upper electrode, located over the insulator 175.

[0031] Unique to the present invention, the first electrode 173, which may comprise a silicide or more particularly a cobalt silicide, may have a reduced surface roughness. For example, the first electrode 173 may have a surface roughness less than about 2.5 nm, or in an exemplary embodiment a surface roughness ranging from about 1 nm to about 2 nm. As the first electrode 173 is formed on the recrystallized polysilicon layer 148 rather than a conventional polysilicon layer or another different material, these reduced surface roughness values are attainable. The first electrode, among others, may also have a thickness that ranges from about 15 nm to about 70 nm.

[0032] While the embodiment of FIGURE 1A illustrates that the recrystallized polysilicon layer 148 is located on the gate electrode layer 143, those skilled in the art understand that this

must not always be the case. For instance, turning to FIGURE 1B, illustrated is an embodiment of the present invention wherein an additional layer 180, or layers, of material interpose the gate electrode layer 143 and the recrystallized polysilicon layer 148. In this instance the first electrode 173 would still be located on the recrystallized polysilicon layer 148, thereby providing the desired surface roughness, however, the recrystallized polysilicon layer 148 would not be located on the gate electrode layer 143, but over the gate electrode layer 143.

[0033] Turning now to FIGURES 2-9, illustrated are cross-sectional views of detailed manufacturing steps instructing how one might, in an advantageous embodiment, manufacture a semiconductor device similar to the semiconductor device 100 depicted in FIGURE 1A. FIGURE 2 illustrates a cross-sectional view of a partially completed semiconductor device 200. The partially completed semiconductor device 200 of FIGURE 2 includes a substrate 210. The substrate 210 may, in an exemplary embodiment, be any layer located in the partially completed semiconductor device 200, including a wafer itself or a layer located above the wafer (e.g., epitaxial layer). In the embodiment illustrated in FIGURE 2, the substrate 210 is a P-type semiconductor substrate; however, one skilled in the art understands that the substrate 210 could be an N-type substrate without departing from the scope of the present invention. In such a case, each of the dopant types described

throughout the remainder of this document would be reversed. For clarity, no further reference to this opposite scheme will be discussed.

[0034] Located within the substrate 210 in the embodiment shown in FIGURE 2 are shallow trench isolation regions 220. The shallow trench isolation regions 220 isolate the semiconductor device 200 from other devices located proximate thereto. As those skilled in the art understand the various steps used to form these conventional shallow trench isolation regions 220, no further detail will be given.

[0035] In the illustrative embodiment of FIGURE 2, also formed within the substrate 210 is a well region 230. The well region 230, in light of the P-type semiconductor substrate 210, would more than likely contain an N-type dopant. For example, the well region 230 would likely be doped with an N-type dopant dose ranging from about  $1\text{E}13$  atoms/cm<sup>2</sup> to about  $1\text{E}14$  atoms/cm<sup>2</sup> and at a power ranging from about 100 keV to about 500 keV. What generally results in the well region 230 having a peak dopant concentration ranging from about  $5\text{E}17$  atoms/cm<sup>3</sup> to about  $1\text{E}19$  atoms/cm<sup>3</sup>.

[0036] Turning now to FIGURE 3, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 2 after formation of a gate structure 310 over the substrate 210. As is illustrated in FIGURE 3, the gate structure 310 includes a gate oxide 320 and a gate electrode stack

330. Unique to the present invention, at this point in the manufacturing process the gate electrode stack 330 comprises a polysilicon gate electrode 333 and an amorphous silicon layer 338.

[0037] To form the gate structure 310 shown in FIGURE 3, a thin gate oxide layer, a thicker polysilicon gate electrode layer and a medium thickness amorphous silicon layer are conventionally deposited on top of one another and then patterned, resulting in the gate structure 310 shown in FIGURE 3. For example, the polysilicon gate electrode layer could be deposited using a pressure ranging from about 100 torr to about 300 torr, a temperature ranging from about 620°C to about 700°C, and a SiH<sub>4</sub> gas flow ranging from about 50 sccm to about 150 sccm. Similarly, the amorphous silicon layer could be deposited using a pressure ranging from about 100 torr to about 300 torr, a temperature ranging from about 450°C to about 550°C, and a SiH<sub>4</sub> gas flow ranging from about 100 sccm to about 300 sccm.

[0038] While the thickness of the gate oxide may vary greatly, in an advantageous embodiment of the present invention the thickness of the polysilicon gate electrode 333 should range from about 50 nm to about 150 nm and the thickness of the amorphous silicon layer should range from about 15 nm to about 75 nm. The thickness of the amorphous silicon layer, however, is particularly dependent on the thickness of the first electrode layer that will subsequently be deposited thereon. For example, if the

subsequently deposited first electrode layer comprises cobalt, it takes approximately 3.6 nm of silicon for every 1 nm of cobalt to form about 3.5 nm of cobalt silicide. If one were wishing to use cobalt silicide as the first electrode, one could use this ratio to choose a particular thickness of the amorphous silicon layer.

[0039] Turning now to FIGURE 4, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 3 after formation of lightly doped extension implants 410 within the substrate 310. The lightly doped extension implants 410 are conventionally formed and generally have a peak dopant concentration ranging from about  $1E19$  atoms/cm<sup>3</sup> to about  $2E20$  atoms/cm<sup>3</sup>. As is standard in the industry, the lightly doped extension implants 410 have a dopant type opposite to that of the well region 230 they are located within. Accordingly, the lightly doped extension implants 410 are doped with a P-type dopant in the illustrative embodiment shown in FIGURE 4.

[0040] Turning now to FIGURE 5, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 4 after formation of conventional gate sidewall spacers 510 and after formation of highly doped source/drain implants 520 within the substrate 210. The formation of the gate sidewall spacers 510, such as Hdd offset spacers, is conventional. Often the gate sidewall spacers 510 comprise a chemical vapor deposition (CVD) oxide and/or nitride material that

has been anisotropically etched.

[0041] Similarly, the highly doped source/drain implants 520 may be conventionally formed. Generally the highly doped source/drain implants 520 have a peak dopant concentration ranging from about  $1\text{E}18$  atoms/cm<sup>3</sup> to about  $1\text{E}21$  atoms/cm<sup>3</sup>. Also, the highly doped source/drain implants 520 should typically have a dopant type opposite to that of the well region 230 they are located within. Accordingly, in the illustrative embodiment shown in FIGURE 5, the highly doped source/drain implants 520 are doped with a P-type dopant.

[0042] Turning now to FIGURE 6, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 5 after subjecting it to a standard source/drain anneal, thereby activating source/drain regions 610. Uniquely, beyond activating the source/drain regions 610, the standard source/drain anneal also converts the amorphous silicon layer 338 to a recrystallized polysilicon layer 620. It is believed that a source/drain anneal conducted at a temperature ranging from about 1000°C to about 1100°C and a time period ranging from about 1 second to about 5 seconds would be sufficient to accomplish both tasks. It should be noted that other temperatures, times, and processes could be used to active the source/drain regions 610 as well as convert the amorphous silicon layer 338 to a recrystallized polysilicon layer 620.

[0043] Turning now to FIGURE 7, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 6 after depositing a first electrode layer 710 on the recrystallized polysilicon layer 620. The first electrode layer 710 in the embodiment shown in FIGURE 7 happens to be a thin cobalt layer, however, other materials that react with silicon to form a silicide could easily be used.

[0044] The first electrode layer 710 of FIGURE 7 was conventionally deposited to a thickness ranging from about 4 nm to about 20 nm. Following the deposition of the first electrode layer 710, an optional capping layer 720 could be deposited thereover. The capping layer 720, which may have a thickness ranging from about 5 nm to about 30 nm, may comprise a number of different materials. For instance, without limiting the present invention to such, the capping layer 720 could comprise titanium or titanium nitride.

[0045] It should be mentioned that prior to forming the first electrode layer 710 the upper surface of the recrystallized polysilicon layer 620 may be cleaned. While it is not entirely imperative, it is believed that a surface cleaning using a diluted HF solution and/or an in-situ plasma (in the same cluster tool as the deposition chamber) would benefit the interface between the recrystallized polysilicon layer 620 and the first electrode layer 710.

[0046] Turning now to FIGURE 8, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 7 after subjecting it to a first rapid thermal anneal (RTA) process and a select etch to remove un-reacted first electrode layer 710 on dielectric surface (such as sidewall and isolation) as well as an optional cap. This first RTA process attempts to cause the first electrode layer 710 to react with the recrystallized polysilicon layer 620 to form a silicide 810. In the instance where the first electrode layer 710 comprises cobalt, the first RTA process causes the cobalt to react with the recrystallized polysilicon layer 620 to form CoSi.

[0047] The first RTA process may be conducted using a variety of different temperatures and times. Nonetheless, it is believed that the first RTA process, in an exemplary embodiment, should be conducted in a rapid thermal processing tool at a temperature ranging from about 400°C to about 600°C for a time period ranging from about 5 second to about 60 seconds. The specific temperature and time period are typically based, however, on the ability to form the silicide 810 to a desired thickness.

[0048] The thickness of the resulting silicide 810 and recrystallized polysilicon layer 620 will most likely be different from the original first electrode layer 710 and original recrystallized polysilicon layer 620, respectively. It is believed that the resulting silicide layer should have a thickness ranging

from about 8 nm to about 40 nm and the remaining recrystallized polysilicon layer 620 should have a thickness ranging from about 7 nm to about 35 nm. This is a result of the silicide 810 consuming at least a portion of the original recrystallized polysilicon layer 620.

[0049] After forming the silicide 810 to a desired thickness, a selective etch is used to remove any un-reacted first electrode layer 710, as well as remove the capping layer 720. The selective etch, among others, could comprise a  $\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2\text{-H}_2\text{O}$  solution. What remains after the selective etch is the silicide 810, which in this embodiment comprises CoSi.

[0050] Turning now to FIGURE 9, illustrated is a cross-sectional view of the partially completed semiconductor device 200 illustrated in FIGURE 8 after subjecting it to a second rapid thermal anneal (RTA) process. This second RTA process attempts to cause the silicide layer 810 to further react with the recrystallized polysilicon layer 620 to form a silicide layer 910. In the instance where the silicide layer 810 comprises CoSi, the second RTA process causes the CoSi to further react with the recrystallized polysilicon layer 620 to form  $\text{CoSi}_2$ . In this instance, the  $\text{CoSi}_2$  has a substantially lower resistivity than the CoSi formed by the first RTA process.

[0051] The second RTA process may also be conducted using a variety of different temperatures and times. Nonetheless, it is

believed that the second RTA process, in an exemplary embodiment, should be conducted in a rapid thermal processing tool at a temperature ranging from about 700°C to about 900°C for a time period ranging from about 5 second to about 60 seconds.

[0052] After completing the silicide layer 910, the manufacture of the capacitor would continue in a conventional manner. Specifically, an insulator and a second electrode would be formed over the silicide layer 910. What results after completion of the capacitor is a device similar to the semiconductor device 100 illustrated in FIGURE 1.

[0053] Turning now to FIGURE 10, illustrated is a graph 1000 illustrating some of the advantages that may be obtained by forming the lower electrode of the capacitor directly on the recrystallized polysilicon layer. Graph 1000 of FIGURE 10 illustrates the sheet resistance ( $R_s$ ) and surface nonuniformity (NU%) for three different situations. Moving from left to right, situation 1 represents an instance where the lower electrode is formed directly on a standard polysilicon layer. Conversely, situation 2 represents an instance where the gate electrode only comprises a recrystallized polysilicon layer, and the first electrode layer is formed directly on the recrystallized polysilicon layer. Situation 3, on the other hand, represents an instance where the gate electrode comprises a gate electrode stack comprising both the recrystallized polysilicon layer and the polysilicon layer, and the first electrode is located

on the recrystallized polysilicon layer and over the polysilicon layer.

[0054] With reference to graph 1000, notice how the sheet resistance and surface nonuniformity are highest for situation 1. For instance, situation 1 shows a sheet resistance of about 32 ohms/sq and a surface nonuniformity of about 8%. In contrast, situation 3 shows a sheet resistance of only about 24 ohms/sq and a surface nonuniformity of only about 5%. Similarly, situation 2 shows a sheet resistance of only about 21 ohms/sq and a surface nonuniformity of about 4%. Clearly then, the use of the recrystallized polysilicon layer has its advantages. It is believed that the smoother surface of the recrystallized polysilicon layer, as compared to the standard polysilicon layer, helps provide these superior results.

[0055] Turning briefly to FIGURE 11, illustrated is a table 1100 showing the surface roughness measured using an atomic force microscope (AFM) of samples similar to situations 1-3 described above. Notice how the surface roughness, in RMS (nm), measures about 3.0000 for situation 1, 1.621 for situation 2, and 2.064 for situation 3. Again, the advantages are apparent.

[0056] One might ask, at least in view of the information provided in FIGURES 10 and 11, why not use only a recrystallized polysilicon gate electrode, similar to situation 2, as it provides the best sheet resistance and surface nonuniformity of the three

situations. While the present invention does not wish to exclude this option, it has been observed that a gate electrode only formed of recrystallized polysilicon has a lower inversion capacitance. It is believed that this lower inversion capacitance is caused by the increased poly depletion, which may be caused by the much slower diffusion of the gate electrode dopant in the recrystallized polysilicon than in the standard polysilicon that consists of columnar grains. This, in effect, hampers the ability of the gate electrode dopant, such as boron, to diffuse to the gate electrode/gate oxide interface. This idea is illustrated in FIGURE 12. The bi-layer stack, that is polysilicon at the bottom of the gate electrode with a layer of recrystallized polysilicon thereover (e.g., situation 3) would address this problem.

[0057] Referring finally to FIGURE 13, illustrated is an exemplary cross-sectional view of a conventional integrated circuit (IC) 1300 incorporating devices 1310 constructed according to the principles of the present invention. The IC 1300 may include devices, such as transistors used to form CMOS devices, BiCMOS devices, Bipolar devices, as well as capacitors or other types of devices. The IC 1300 may further include passive devices, such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of devices and their manufacture. In the particular embodiment illustrated in FIGURE 13, the IC 1300

includes the devices 1310 having dielectric layers 1320 located thereover. Additionally, interconnect structures 1330 are located within the dielectric layers 1320 to interconnect various devices, thus, forming the operational integrated circuit 1300.

[0058] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.